UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,402	03/12/2004	Nobutaka Kitagawa	250330US2S	6011

22850 7590 08/24/2006

C. IRVIN MCCLELLAND
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
ROMAN, LUIS ENRIQUE	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,402	KITAGAWA, NOBUTAKA	
	Examiner	Art Unit	
	Luis Roman	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ito et al. (US 6683767) in view of Ker et al. (US 5637900) and English et al. (US 5745323).

Regarding claims 1-6 Ito et al. discloses a semiconductor integrated circuit (Fig. 1 element 10) comprising: an inner circuit (Fig. 1 element 2) driven by a single power voltage (Fig. 1 element L20<Vext>); and protective circuits (Col. 2 lines 15-16 & Fig. 1 element 2).

Ito et al. does not specifically disclose a first protective circuit which protects the inner circuit from a surge, wherein the inner circuit includes: a high voltage-proof circuit section constituted of a first MOS transistor; a low voltage-proof circuit section constituted of second MOS transistor including gate insulating film thinner than that of the first MOS transistor; and a second protective circuit directly connected to the low voltage-proof circuit section to protect the second MOS transistor from the surge.

Ker et al. discloses an ESD protection circuitry wherein the inner circuit includes: a high voltage-proof circuit section constituted of a first MOS transistor (Fig. 6 element P3); a low voltage-proof circuit section constituted of second MOS transistor including gate insulating film thinner than that of the first MOS transistor (Fig. 6 element P1); and a second protective circuit directly connected to the low voltage-proof circuit section to protect the second MOS transistor from the surge (Fig. 6 elements P4, P5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Ito et al. device with the Ker et al. teachings because it will provide a protection from four different ESD stress modes by providing more discharging paths (Ker et al. <Abstract>).

Ito et al. in view of Ker et al. does not disclose a first protective circuit, which protects the inner circuit from a surge.

English et al. teaches a thick oxide MOS protecting another thick oxide MOS (Fig. 6 elements 122, 232).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Ito et al. in view of Ker et al. device with the English et al. teachings because it provides an enhance ESD protection to the circuit (English et al. <Col.1 lines 54-61>).

Ito et al. further discloses wherein a low voltage-proof circuit section is driven by an inner power voltage, which is obtained by stepping down the single power voltage (Col. 2 lines 16-25).

Ker et al. further discloses wherein the second MOS transistor is a device, which directly receives the inner power voltage (Fig. 6 elements P1, VDD).

Ker et al. further discloses wherein the second MOS transistor is a device which directly receives data from the high voltage-proof circuit section (Fig. 6 elements P1 getting data from path 155 thru gate 145).

Ker et al. further discloses wherein the second protective circuit constituted of a diode or diode-connected MOS transistor, and a clamp voltage by the diode or the diode-connected MOS transistor is larger than a maximum value of a voltage range at the time of a usual operation in the low voltage-proof circuit section (Col. 8 lines 5-33).

FIG. 1

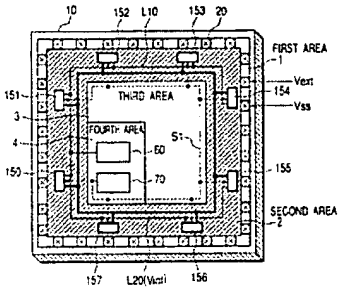
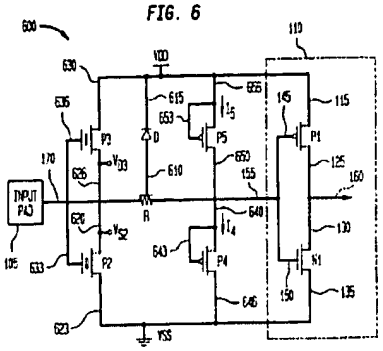


FIG. 6



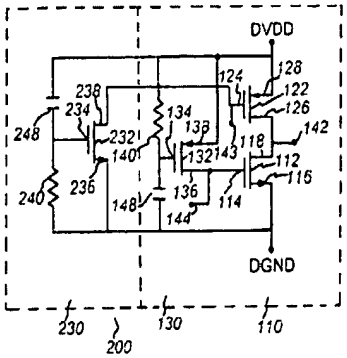
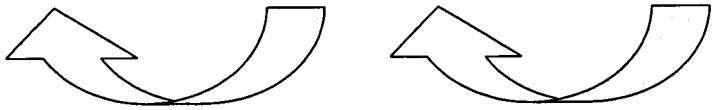


Fig. 6

Ito et al. Ker et al. English et al.



Regarding claims 7-12 Ito et al. in view of Ker et al. and English et al. discloses a semiconductor integrated circuit (Ito et al. <Fig. 1 element 2>) comprising: a high voltage-proof circuit section constituted of a first MOS transistor and driven by a single power voltage (English et al. <Fig. 6 element 122>); and a first protective circuit which protects the high voltage-proof circuit section from a surge (English et al. <Fig. 6 element 232>), wherein the high voltage-proof circuit section includes: a low voltage-proof circuit section constituted of a second MOS transistor including a gate insulating film thinner than that of the first MOS transistor (Ker et al. <Fig. 6 element P1>); and a second protective circuit directly connected to the low voltage-proof circuit section to protect the second MOS transistor from the surge(Ker et al. <Fig. 6 elements P4, P5>).

Ito et al. further discloses wherein the low voltage-proof circuit section is driven by an inner power voltage obtained by stepping down the single power voltage (Col. 2 lines 16-25).

Ker et al. further discloses wherein the second MOS transistor is a device, which directly receives the inner power voltage (Fig. 6 elements P1, VDD).

Ker et al. further discloses wherein the second MOS transistor is a device, which directly receives data from the high voltage-proof circuit section (Fig. 6 elements P1 getting data from path 155 thru gate 145).
Ker et al. and English et al. further discloses wherein the low voltage-proof circuit section exchanges data (Ker et al. <Fig. 6 elements P1, path 155>) with respect to the high voltage-proof circuit section (English et al. <Fig. 6 elements 122, path 142).
Ker et al. further discloses wherein the second protective circuit is the high constituted of a diode or a diode-connected MOS transistor, and a clamp voltage by the diode or the diode-connected MOS transistor is larger than a maximum value of a voltage range at the time of a usual operation in the low voltage-proof circuit section (Col. 8 lines 5-33).

Regarding claims 13-20 Ito et al. in view of Ker et al. and English et al. discloses a semiconductor integrated circuit (Ito et al. <Fig. 1 element 2>) comprising: a first inner circuit constituted of a first MOS transistor and driven by a first power voltage (English et al. <Fig. 6 element 122>); a second inner circuit constituted of a second MOS transistor including a gate insulating film thinner than that of the first MOS transistor (Ker et al. <Fig. 6 element P1>) driven by a second power voltage lower than the first power voltage to exchange data with respect to the first inner circuit (Ito et al. <Col. 2 lines 16-25>); a first protective circuit directly connected to the first inner circuit to protect the first MOS transistor from a surge (English et al. <Fig. 6 element 232>); and a second protective circuit directly connected to the second inner circuit to protect the second MOS transistor from the surge (Ker et al. <Fig. 6 elements P4, P51>).
Ker et al. further discloses wherein the second MOS transistor is a device which directly receives the second power voltage (Fig. 6 elements P1, VDD).
Ker et al. further discloses wherein the second MOS transistor is a device which directly participates in the exchange of the data (Fig. 6 elements P1 getting data from path 155 thru gate 145).
Ker et al. further discloses wherein the second protective circuit is directly connected to the second MOS transistor (Fig. 6 elements P1, P4, P5).

English et al. teaches an ESD complementary protection with a resistor and a capacitor, which clamps the surge with a time constant smaller than a transition time of a signal to effectively operate (Col. 6 lines 2-19 & Fig. 6 elements 240, 248).

Ker et al. further discloses wherein the second protective circuit is constituted of a diode or a diode-connected MOS transistor, and a clamp voltage by the diode or the diode-connected MOS transistor is larger than a maximum value of a voltage range at the time of a usual operation in the second inner circuit (Col. 8 lines 5-33).

Ker et al. further discloses wherein the second protective circuit is constituted of an analog switch (Fig. 6 element P5).

English et al. discloses wherein the first protective circuit is directly connected to an external terminal (Fig. 6 elements132, VDD), and the second protective circuit (Ker et al. <Fig. 6 elements P4, P5>) is not directly connected to the external terminal (Ito et al.<implicitly disclosed since there is a step-down device between the two protective circuits - Col. 2 lines 16-25>).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luis E. Román whose telephone number is (571) 272 – 5527. The examiner can normally be reached on Mon – Fri from 7:15 AM to 3:45 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from Patent Application Information Retrieval (PAIR) system.

Status information for unpublished applications is available through private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luis E. Román
Patent Examiner
Art Unit 2836

LR/081806

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800